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FOR

ANALOG CONTROL INTEGRATED FET BASED VARIABLE ATTENUATORS

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ANALOG CONTROL INTEGRATED FET BASED VARIABLE ATTENUATORS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of analog attenuators.

2. Prior Art

Variable analog attenuators are commonly used in applications which require signal level control, such as, by way of example, in radio frequency (RF) automatic gain control (AGC) circuits. Typically discrete PIN diodes are used for this purpose. A PIN diode differs from an ordinary PN diode in that there is an intrinsic semiconductor region (I) between the P and N doped regions of the diode. When a forward bias is applied to the diode, a large number of electrons and holes are created in the intrinsic region, allowing forward conduction. If the bias is suddenly removed, these charge carriers will not immediately recombine, and thus will not immediately stop the conduction current. Thus PIN diodes will conduct high frequency signals superimposed on a bias current without much distortion, even for large signals that would cause a momentary reversal of the PIN diode current. However the present invention

performs the desired function, but being part of an integrated circuit, is smaller, less expensive, has less power consumption and provides constant attenuation versus control voltage slope when compared to conventional discrete PIN diode based analog attenuators.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1a and 1b show simplified diagrams of integrated FET analog attenuators in accordance with the present invention.

Figures 1c and 1d show two specific possible configurations for the voltage controlled variable resistors for the attenuators of Figures 1a and 1b.

Figures 2a and 2b show a voltage controlled variable resistor and a curve illustrating the total resistance R_T versus the control voltage Vc for that voltage controlled variable resistor, respectively.

Figures 2c and 2d show another voltage controlled variable resistor and a curve illustrating the total resistance R_T versus the control voltage Vc for that voltage controlled variable resistor, respectively.

Figures 3a and 3b present schematics of a π-attenuator and a T-attenuator, respectively, in accordance with the present invention.

Figure 3c presents a curve illustrating the characteristics of insertion loss or attenuation versus the control voltage Vc for the circuits of Figures 3a and 3b.

Figures 3d and 3e illustrate a multiple stage attenuator (multiple attenuators in cascade) with a proper control signal for each variable resistor, and the constant slope of attenuation (in dB) versus control voltage Vc that can be obtained with such a multiple stage attenuator, respectively.

Figures 4a and 4b generally illustrate the control signal for each variable resistor as generated from an attenuation control voltage (Vctrl), and a set of sample control signals versus Vctrl, respectively.

Figures 4c, 4d and 4e present a diagram illustrating how the sample control signals of Figure 4b may be generated, a circuit that may be used for each of the amplifiers (Aa through Az) of Figure 4c, and a graph illustrating the control signals Vcn and VcN generated by the circuits of Figures 4c and 4d, respectively.

Figures 5a and 5b present a π-attenuator element or stage in accordance with the present invention and a graph illustrating its temperature dependence, respectively.

Figures 5c and 5d illustrate how the circuit of Figure 5a may be compensated to reduce the temperature dependence at the lower attenuation levels by adding small transistors Q4 and Q5, and the effect of that compensation, respectively.

Figures 6a, 6b and 6c illustrate two different ways how the circuit of Figure 5a may be temperature compensated at high attenuation, and the resulting insertion loss variation with temperature, respectively.

Figure 7a shows a transistor, together with its intrinsic parasitic capacitances, biased in its linear region.

Figures 7b through 7d graphically illustrate large signal effects on the transistor of Figure 7a.

Figure 8a illustrates the transistor of Figure 7a, but with high impedance (relative to the capacitive impedances at the RF frequency of interest) gate bias and body bias connections.

Figures 8b and 8c graphically illustrate large signal effects on the transistor of Figure 7a as biased as in Figure 8a.

Figures 9a and 9b illustrate possible control sequences of the attenuator for lower attenuation and higher attenuation states, respectively.

Figure 10 is a circuit diagram for an exemplary embodiment of attenuator in accordance with the present invention.

Figure 11 presents an exemplary curve of attenuation vs attenuation control voltage for an attenuator in accordance with the present invention.

Figure 12 presents exemplary curves of attenuation vs attenuation control voltage at three different temperatures for an attenuator in accordance with the present invention.

Figure 13 illustrates a differential or double ended variable attenuator in accordance with the present invention.

Figure 14 illustrates an alternate embodiment differential or double ended variable attenuator in accordance with the present invention.

Figure 15 illustrates a still further alternate embodiment differential or double ended variable attenuator in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

I. Analog Control Integrated Field-Effect-Transistor Based Attenuator

Figures 1a and 1b show simplified diagrams of integrated FET analog attenuators in accordance with the present invention. The attenuation or insertion loss of these analog attenuators is controlled by the impedance of the voltage controlled variable resistors shown in Figures 1a and 1b. There are several possible configurations for the voltage controlled variable resistors. Two examples are shown in Figures 1c and 1d. The control signal Vc (also see Figures 1a and 1b) controls the on-resistance of the transistors to change the total impedance R_T of the variable resistors by turning the transistors on, off and partially on/off. For the configuration of Figure 1c, the total resistance when the FET Q1 is on is $R_T = R + R_{ON}$, where R_{ON} is the on resistance of the FET Q1, and the total resistance will be very large when the FET is off. For the configuration of Figure 1d, the total resistance when the FET Q1 is on is $R_T = (R)(R_{ON})/(R + R_{ON})$ and the total resistance when the FET is off is R.

By changing Vc to alter the on-resistance of the transistors, the total resistance R_T can be varied. The examples of total resistance R_T versus the control voltage Vc for the configuration of Figure 1d (see also Figure 2a) is

illustrated graphically in Figure 2b. Figure 2c presents still another FET variable resistance circuit with FET transistors Q1n and Q2n. Transistor Q2n is controlled by the voltage VcN, where VcN is an inverse or opposite (as shall be more fully illustrated later herein) of the voltage Vcn controlling the transistor Q1n. As transistor Q1n is turned on, transistor Q2n is turned off, and vise versa. The examples of total resistance R_T versus the control voltage Vcn for the configuration of Figure 2c is illustrated graphically in Figure 2d. As shown in Figures 2b and 2d, total resistance R_T versus control voltage Vcn can be roughly divided into three states, namely a higher impedance state, a lower impedance state and a transition state. By using these three states of variable resistors, an analog voltage control π-attenuator (Figure 1a) or a T-attenuator (Figure 1b) can be developed.

Schematics of a π-attenuator and a T-attenuator in accordance with the present invention are shown in Figures 3a and 3b, respectively. Each variable resistor in the attenuators should be properly configured by using different types of variable resistors, such as those shown in Figures 1c, 1d and/or 2c in order to perform the desired function for the attenuator. Figure 3c generally shows the characteristics of insertion loss or attenuation versus the control voltage Vc for the circuits of Figures 3a and 3b.

The attenuation can be controlled by changing Vc to achieve the desired attenuation level. However as illustrated in Figure 3c, the slope of attenuation versus the control voltage V_C during transition is not constant. This is mainly due to the nonlinear total resistance R_T versus control voltage Vc of the variable resistors. In addition, the transition is usually sharp.

The non-constant slope of attenuation and sharp transition versus control voltage as shown in Figure 3c is usually not desired. One possible solution for that is to use multiple attenuators in cascade (a multiple stage attenuator) as shown in Figure 3d, with a proper control signal for each variable resistor. Typically in such an attenuator, all series variable resistors will be of the same circuit configuration and device sizing, and all shunt variable resistors will be of the same circuit configuration and device sizing, except the first and last shunt resistors, though this is not a limitation of the invention. By using this configuration and control, a constant slope of attenuation (in dB) versus control voltage Vc can be obtained, as shown in Figure 3e. The key to achieve this constant slope during transition are the individual control signals for each of the variable resistors, Vca, Vcb . . . Vcy, Vcz (no specific number of stages implied). The control signal for each variable resistor is generated from an

attenuation control voltage (Vctrl), as shown schematically in Figure 4a. A set of sample control signals versus Vctrl is shown in Figure 4b. With a set of control signals like this applied to the attenuator of Figure 3d, attenuation versus Vctrl having a constant slope as shown in Figure 3e is achievable.

The control signals Vca, Vcb . . . Vcy, Vcz may be generated from the control voltage Vctrl using a circuit such as that shown in Figure 4c. In this embodiment, a resistor string is used to divide down a reference voltage Vref to provide a plurality of lower voltages Refa, Refb, ..., Refz, each providing one input to a respective low gain, differential input, differential output amplifier Aa, Ab, ..., Az. The second input to each differential amplifier is the control signal Vctrl, and the outputs are the differential signals Vca,VcA, Vcb,VcB, ..., Vcz,VcZ. When the differential input to any one amplifier is zero, the differential output is preferably zero, with the two outputs preferably being at midrange, as may be seen in Figure 4c. For good temperature and supply voltage rejection, Vref should be temperature and supply voltage stable, such as, by way of example, may be provided by a band gap reference.

One suitable circuit for the amplifiers Aa, Ab, ..., Az may be seen in Figure 4d. In this circuit, transistors Q1

and Q2 have source degeneration resistors R to reduce the gain of the differential pair and to better linearize the output. The drain currents are mirrored to load resistors R_L to provide the outputs Vcn, VcN. Current source I, preferably also temperature and supply voltage independent, determines the combined currents through the transistors. When Vctrl < Ref - IR, transistor Q1 will be off, and all the current I will flow through transistor Q2. When Vctrl > Refn + IR, transistor Q2 will be off, and all the current I will flow through transistor Q1. However, when (Refn - IR) < Vctrl < (Refn + IR), then Vcn and VcN will vary nearly linearly between their respective extremes (zero and IR_L in this exemplary circuit) with a slope of $R_L/2R$. This is illustrated in Figure 4e. The same circuit may be realized using other types of transistors, such as MESFETs, JFETs or bipolar junction transistors, or other circuits may be used as desired.

II. Temperature Dependence Reduction

Now referring to Figures 5a and 5b, a π-attenuator element in accordance with the present invention and a graph illustrating its temperature dependence may be seen. The on resistance of a FET is temperature dependent, and increases with increasing temperature. Consequently with transistor Q1 on and transistors Q2 and Q3 off, the minimum insertion loss

(IL) for the circuit will be lower for lower temperatures because of the lower combined resistance of resistor R1 and transistor Q1. With transistor Q1 off and transistors Q2 and Q3 on, the maximum insertion loss (IL) for the circuit will be higher for lower temperatures because of the lower series resistance of resistor R2 and transistor Q2, and resistor R2 and transistor Q3. The circuit may be compensated to reduce the temperature dependence on the lower attenuation levels by adding small transistors Q4 and Q5 compared to transistor Q1 as shown in Figure 5c, and controlling them with the same control signal as is used to control transistor Q1. Transistors Q4 and Q5 introduce some additional loss, but in return, provide fairly high resistance paths to ground that vary with temperature to offset or compensate for the effect of the temperature variation of the resistance of transistor Q1 when it is on. The result is illustrated in Figure 5d, wherein it may be seen that the temperature dependence of the insertion loss (IL) for low insertion loss is minimal, though the temperature dependence at high attenuation remains.

For temperature compensation at high attenuation for the circuit of Figure 5a, either transistor Q4 may be added, as shown in Figure 6a, or transistor Q5 may be added as shown in Figure 6b. In Figure 6a, transistor Q4 would be a large transistor (low on resistance) compared to transistors Q2 and Q3 which, when on, would compensate for the temperature

variation of the on resistance of transistors Q2 and Q3. However, timing of the control of transistor Q4 is critical, so this circuit is not preferred for analog attenuators. In the circuit of Figure 6b, transistor Q5 is a small transistor compared to transistors Q2 and Q3, and may be controlled by the same control signal as transistor Q3 to compensate for the temperature sensitivity of transistor Q3. In either case, the insertion loss variation with temperature will be as illustrated in Figure 6c.

Temperature compensation for both high and low attenuation may be achieved by combining the foregoing circuit techniques. However, the chip area needed may become larger than desired, particularly when the following solution for higher power handling and linearity of FET attenuators are implemented. Consequently, compromises may often be made to achieve a good balance between the chip area required and performance needed. By way of example, in a closed loop automatic gain control application, the loop itself may provide adequate temperature compensation.

III. Higher Power Handling and High Linearity FET Attenuators

Two of the key figures of the merit of an attenuator are the power handling capability, measured by P1dB (power in dB at the fundamental frequency), and the linearity, mainly

measured by IP3 (third harmonics caused by nonlinearities). In most cases for integrated circuits, P1dB and IP3 can be theoretically related to be 10 dB apart. Thus, optimizing P1dB also optimizes IP3 in most cases.

Figure 7a shows a transistor, with its intrinsic parasitic capacitances, biased in its linear region. The gate (V_G) and body (V_B) nodes of the transistor are AC grounded in this case. The drain voltage may have a DC component V_D plus a signal component v_d. As shown in Figure 7b, with a large AC signal v_d applied to the drain of the transistor, the large AC signal v_d on top of the DC bias voltage V_D at the drain node can either swing above the gate voltage V_G or swing below the body voltage V_B at some portion of the cycle. This can either turn off the transistor when it should be on as shown in Figure 7c, or at least fluctuate the on-resistance of the transistor. These limit the P1dB and IP3 of the transistors. Figure 7c also shows that at some portion of the cycle, the voltage drop across the gate-to-drain/source/body oxide could be too high. This high voltage drop across the gate oxide can result in dielectric reliability issues.

Similarly, as shown in Figure 7d, the drain-to-body voltage may swing enough below ground voltage to forward bias the drain-to-body junction at some portion of the cycle.

This forward biased drain-to-body junction causes signal distortion, and thus limits P1dB and IP3. This forward biased junction may also trigger latch-up for circuits implemented using bulk silicon substrate technologies.

The requirement of reverse biased junction diodes, the unintentionally turned on or turned off transistor and also the dielectric reliability limitations all limit the power handling capability of the transistor. One approach to increase the power handling capability of the transistor is to use high impedance (relative to the capacitive impedances at the RF frequency of interest) gate bias and body bias connections as shown in Figure 8a. The gate and body resistors R_G and R_B represent high impedance devices (substantially higher impedance than the respective parasitic capacitances at the frequencies of the AC signal) to provide AC isolation between the transistor gate and source nodes and their DC supply and ground, respectively. The existence of the high impedance device R_G between the gate node and its bias allows the AC signal to be coupled to the gate node from the input through the parasitic capacitances, as illustrated in Figure 8b. As shown in Figure 8c, this coupled AC signal prevents the relative gate-to-drain voltage V_{GD} (AC voltages plus DC voltages $(V_G + v_g) - V_D + v_d)$) of the transistor from fluctuating by causing the AC variation of the gate to drain

voltage v_{gd} to be negligible. In Figure 8a, the body resistor is shown referenced to ground, though the same can be referenced to some other reference voltage provided care is taken to never forward bias either the source-body or the drain-body diode into conduction.

A similar mechanism also applies to the source/drain-to-body voltage. The existence of the high impedance devices, R_G and R_B in this case, maintains the DC bias point of the transistor even with a large AC signal at the source and drain nodes of the transistor. This, in turn, greatly enhances the P1dB and also the IP3 of the transistors.

Figure 7 and Figure 8 provided examples for transistors biased in the linear region. This means that the DC source drain voltage (the DC source-to-drain bias) V_{DS} of the transistors is low, preferably substantially zero. The high impedance coupling of the gate and body allow the gate and body to vary with the signal at the signal frequencies, so that the gate and body will swing or float with the signal. Thus while the drain source (drain-to-source) voltages of the FETs will vary with the signal when in the transition region, the variation will be within the linear region, so that the instantaneous current through a FET will be proportional to the instantaneous AC component of the voltage across the FET (like a resistor). To achieve a low or substantially zero

DC source drain voltage on the transistors, the input and output voltages of an attenuator (or individual resistor subsequently described) should be balanced signals. By way of example, for a single ended attenuator such as shown in Figure 3d, balanced signals may be obtained by making the common connection equal to the average input (and output) signal, or by AC (capacitively) coupling the input and output of the attenuator. For a differential attenuator like that of Figure 13 to be described, the DC or average source drain voltage should automatically be substantially zero.

For small signal variable resistors and attenuators, the FET or FETs should be biased to operate in the linear region, or preferably with a substantially zero DC or average source drain voltage, but the gate and/or body may not need to be AC floated as described above.

For high P1dB and IP3, it is also important for the transistors to remain off in the presence of large signals when biased in the off-state. However the concept demonstrated in Figure 7 and Figure 8 is also applicable to transistors biased in the off-state.

Given the technique to improve transistor P1dB and IP3, the P1dB and IP3 of the variable resistors schematically shown in Figure 1 can be higher. This increases the P1dB and IP3 of the attenuator shown in Figure 3d. However, the worst

case P1dB and IP3 of the variable resistor does not occur when the transistors are biased in fully on or fully off regions. It was usually limited by a transistor biased in the transition from on to off states or the reverse transition. As shown in Figures 2b and 2d, with a slight Vc change, the effective impedance of the variable resistor in the transition region can change by a lot compared to the other two states (on and off) of the transistor. Because of this, the sequence of the control signals as shown in Figure 4b has a substantial effect on the P1dB and IP3 of this attenuator.

Figures 9a and 9b show a possible control sequence of the attenuator in both lower attenuation and higher attenuation states. For minimum attenuation (Figure 9a), the variable resistors in series between the IN and OUT nodes are in the low impedance state L (the transistors are on) and the variable resistors coupled to ground are in the high impedance state H (the transistors are off). The attenuation is increased by switching the variable resistors, thus the transistors, from lower impedance state (L) to higher impedance state (H) through transition region (T), or H to T to L, in a controlled sequence. The control sequence starts from the variable resistors near the IN node and progresses to those near the OUT node in this example. As shown in Figure 9a, under lower attenuation conditions, the variable

resistors near the IN node are shifted into transition T, and this limits the input P1dB and IP3 of the attenuator under lower attenuation conditions.

At higher attenuation, the variable resistors near the IN node will have been switched to either H or L and the P1dB and the IP3 are limited by the variable resistors in the T region near the OUT node, as shown in Figure 9b. The output P1dB in both lower attenuation and higher attenuation cases is similar if the minimum insertion loss of the attenuator is negligible. However, the input P1dB (output P1dB plus attenuation) under higher attenuation will be higher. If the transition sequence from IN to OUT is reversed, the input P1dB at low attenuation can be higher but the input P1dB at higher attenuation will be similar and thus the output P1dB reduces to the input P1dB minus the attenuation. This is much lower than the previous case and is usually not desired.

Now referring to Figure 10, a circuit diagram for an exemplary embodiment of attenuator in accordance with the present invention may be seen. In this attenuator, the control signals are Vc1 through Vc7 and their complements Vc1B through Vc7B. "Each" shunt transistor to AC ground is actually comprised of four transistors in series, mainly to improve the power handling and linearity due to unintentional turning on/off of shunt transistors at high input power.

Also, this improves dielectric reliability at high input power by reducing the voltage drop across each transistor. The body of each of these transistors is coupled through a high impedance resistor (compared to the impedance of the parasitic capacitances at the RF frequency) to AC ground as shown. The main attenuator control transistors are the shunt transistors and the transistors controlled by the control signals Vc1 through Vc7, the transistors in parallel with the transistors controlled by the control signals Vc1 through Vc7 being small transistors to compensate for the temperature sensitivity of the on resistance of the shunt transistors (Figure 6b), the specific attenuator shown in Figure 10 not further incorporating temperature compensation.

In any attenuator in accordance with the present invention, the number of stages used will mainly depend on the desired dynamic range, attenuation slope, smoothness of the slope, minimum insertion loss, power handling capability and linearity. As an example, for 15 dB of dynamic range with ~1.2 dB minimum insertion loss, 38 dBm P1dB and a constant transition slope at 900 MHz, 7 stages have been used. For the same 15 dB dynamic range with ~0.7 dB insertion loss, 25 dBm P1dB and near-constant transition slope (with some bumps) at 900 MHz, only three stages were used. Also in most cases, the resistors and the transistors in the series branches will not be the same as the ones in

the shunt branches, but all the resistors and transistors in the series branches for each stage are usually the same, and all the resistors and transistors in the shunt branches for each stage are usually the same, except the first and last shunt branches. This is good for input/output impedance matching. However in some cases where a taper attenuation curve for specific application is needed, the resistors and transistors in each stage will not be the same.

Figure 11 presents an exemplary curve of attenuation vs attenuation control voltage for an attenuator in accordance with the present invention. This curve shows the attenuation versus attenuation control voltage for an analog attenuator consisting of seven sections. The ripple in the plot is contributed from each section of the attenuator. The slope of attenuation versus control voltage is monotonic and semi-constant. The ripple and slope can be improved by adding more sections, the trade off being the minimum insertion loss of the attenuator.

Figure 12 presents exemplary curves of attenuation vs attenuation control voltage at three different temperatures for an attenuator in accordance with the present invention. The three curves in this plot show the attenuation curve at -40, 25 and 85°C, respectively. This attenuator includes high attenuation temperature compensation to reduce the

attenuation variation to +/- 0.5 dB. If the temperature compensation is not utilized, the attenuation variation versus temperature at high attenuation is expected to be around +/- 1.5 dB.

Figure 13 illustrates a differential or double ended variable attenuator in accordance with the present invention. This circuit, like the single ended attenuator of Figure 3d, may use any of the variable resistances disclosed herein, or variable resistances of other circuit configurations using one or more FETs as desired, provided the FETs have their bodies coupled to ground or some other reference voltage through an impedance, typically a resistance, that is higher than the impedance of the body parasitic capacitances at the signal frequencies to be attenuated, and have their gates coupled to a control voltage through an impedance, also typically a resistance, that is higher than the impedance of the gate parasitic capacitances at the signal frequencies to be attenuated. Preferably, but not necessarily, the impedances coupling the body to its reference voltage and the gate to its control voltage are an order of magnitude (10 times) the associated parasitic impedances.

Figure 14 illustrates an alternate embodiment differential or double ended variable attenuator in accordance with the present invention. This embodiment

differs from the embodiment of Figure 13 in that the variable resistors at the ends of the attenuator are series variable resistors, not shunt variable resistors. In that regard, the phrase alternate series and shunt variable resistors as used in the claims to follow does not suggest either particular type of variable resistor (series and shunt) at the ends of an attenuator, single ended or differential, or for that matter, that the two ends of the attenuator have the same type of variable resistor, though that will usually be the case.

Figure 15 illustrates a still further alternate embodiment differential or double ended variable attenuator in accordance with the present invention. This embodiment is similar to that of Figure 13, though with each shunt variable resistor being comprised of two shunt variable resistor portions with a common mode AC ground between each pair of shunt variable resistor portions. Each shunt variable resistor portion in each pair would normally be identical variable resistor portions, with each variable resistor portion in a respective pair of variable resistor portions being coupled to the same respective control voltage.

It should be noted that the present invention has been disclosed in conjunction with analog attenuators having a substantial attenuation range. However the principles of the

present invention are also applicable to single variable resistances as well as single stage π-attenuators and T-attenuators, which may be useful in applications that do not require a wide range of control, or where a variable resistor is needed for some other purpose. Also, in some applications, it may be appropriate to distribute the stages of a multistage attenuator along an analog signal path, using one or more stages at various locations along the signal path. This could preserve the overall attenuation range, though allow each analog signal processing element to operate at its optimum signal to noise ratio.

There have been disclosed herein analog control integrated FET based variable resistances and attenuators, as well as methods and circuits for temperature compensation and for minimization of large signal distortion. The advantages of these integrated attenuators include smaller size, less expensive, less power consumption and constant attenuation versus control voltage slope compared to conventional discrete PIN diode based analog attenuators. These attenuators can be integrated in most of the available integrated circuit technologies. Because of this, this invention enables the integration of the analog control variable attenuator with other circuits and thus greatly reduces the size and cost for circuits requires this function.

While certain preferred embodiments of the present invention have been disclosed and described herein, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention. Similarly, the various aspects of the present invention may be advantageously practiced by incorporating all features or various sub-combinations of features.